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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,651	02/04/2004	Dong-Kil Shin	9898-341	5815

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	
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12/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/772,651	SHIN ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on October 3, 2007.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (US 6,133,637) in view of Kondo et al. (JP 63-240053 A), Scranton et al. (US 6,099,783), and Nakayama et al. (US Pub. 2002/0004258 A1).

In re claim 1, Hikita et al. shows (fig. 9) a multi-chip package comprising: at least two semiconductor chips (14 and 16) vertically mounted on a substrate (12a) and encapsulated with a mold resin (22); and a soft element (elastomer or epoxy resin 18) located between at least one of the at least two semiconductor chips and the mold resin, the soft element being more elastic and flexible than the mold resin (col. 5, lines 24-38). Because the soft element of Hikita is formed of the same materials and structure as the applicant's claimed invention, it is also inherently configured to reduce the constrictive force of the encapsulant on the surface. In re limitation of the soft element being "adapted" to relieve stress, it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires

the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

However, Hikita does not clearly disclose that the soft element relieves stress between the chips and the mold resin. Kondo discloses (abstract and fig. 2) a soft element (flexible material 9) formed on an entire upper surface and side surface of a chip (1). The soft element is formed between the chip and the mold resin (3) to protect the package from internal stress. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Hikita by forming the soft element on the top surface of the chip and between the chip and the mold resin as taught by Kondo to protect the package from internal stress.

Hikita and Kondo show all of the elements of the claims except the soft element being an elastomer or epoxy resin without a filler. It is well known in the art that encapsulant materials can be formed with or without fillers to form the encapsulant having a desired property (adhesive property, hardness property, etc.) However, Scranton et al. discloses (col. 17, lines 56-61) that an epoxy resin material may be formed without a filler to so that the resin has a putty-like property. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the soft element of Hikita and Kondo by using an encapsulant material having no filler as taught by Scranton to form a soft element having a putty-like property.

Hikita, Kondo and Scranton show all of the elements of the claims except the side surface of the two semiconductor chips being coplanar. Such a limitation is not patentably distinguishable over the cited art because two vertically stacked

semiconductor chips being identical, or having the same size would have side surfaces that are coplanar. However, Nakayama et al. shows (fig. 2) a device having two semiconductor chips (30, 40) that are vertically stacked and have side surfaces that are coplanar. The chips allows mounting resin to extend to both sides of the chip to mount them to the substrate together [0111-0112]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Hikita, Kondo and Scranton by forming the chips having coplanar side surfaces as taught by Nakayama to extend resin along both sides of the chip for mounting to a substrate.

In re claims 2 and 3, Hikita et al. shows (fig. 9) a soft element (epoxy resin 26) contacts an entire surface of the side or a portion of the side of the semiconductor chips.

In re claims 4 and 5, Kondo shows (fig. 2) that the soft element contacts the entire upper surface of the chip or a portion of the upper surface of the chip (as shown in figures 1 or 3).

In re claim 6, Hikita et al. discloses (col. 5, lines 24-28) that an adhesive is applied for adhesion between the substrate and the semiconductor chips. Because the soft element of Hikita is formed of the same materials and structure as the applicant's claimed invention, it is also inherently configured to increase vertical mobility of the semiconductor chips against a load of the adhesive applied to the semiconductor chips upon cooling.

In re claim 7, Hikita et al. discloses (col. 6, lines 24-38 and col. 6, lines 25-33) that the soft element comprises elastomer or epoxy resin.

In re claim 21, although Hikita shows that a soft element is disposed between the two chips in figure 10, Hikita shows in figure 49 that there is no soft element between the chips, and when combined with Kondo, the soft element (9) of Kondo would be formed on the uppermost chip and not between the two chips of Hikita. Kondo shows that the soft element is not disposed between the chip (1) and lead frame (2).

In re claim 23, Nakayama shows that a resin (74) covers substantially the entire side surfaces of the two chips. When combined with Kondo, the soft element of Kondo would be applied to both chips and cover the entire side surfaces of those chips.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (US 6,133,637) in view of Kondo et al. (JP 63-240053 A), Scranton et al. (US 6,099,783), and Nakayama et al. (US Pub. 2002/0004258 A1) as applied to claim 1 above, and further in view of Derderian (US 6,569,709 B2).

In re claims 8 and 9, Hikita, Kondo, Scranton, and Nakayama show all of the elements of the claims except the solder balls as terminals for connecting the package to an external circuit and the substrate being a PCB. Derderian et al. shows (fig. 1) a package having vertically stacked semiconductor chips (30a and 30b) and a soft element formed between them. The package is a PCB (20) having solder balls (14) formed as terminals for connecting the package to an external circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify the package of Hikita, Kondo, Scranton, and Nakayama by using solder balls as terminals as taught by Derderian to connect the package to an external circuit.

Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. (US 6,215,182 B1) in view of Kondo et al. (JP 63-240053 A), Scranton et al. (US 6,099,783), and Nakayama et al. (US Pub. 2002/0004258 A1).

In re claim 10, Ozawa et al. shows (fig. 5) a device comprising at least two semiconductor chips (22-24) stacked on a substrate; and an encapsulant (26) covering the at least two semiconductor chips. Ozawa shows all of the elements of the claim except the soft element formed on a surface of at least one of the two chips but not on surfaces between the two chips. Kondo discloses (abstract and fig. 2) a soft element (flexible material 9) formed on an entire upper surface and side surface of a chip (1). The soft element is more flexible than the encapsulant and is formed between the chip and the mold resin (3) to protect the package from internal stress. When combined with Ozawa, the soft element would not be formed between the at least two semiconductor chips since Ozawa relies on a film adhesive (38) to secure the chips to each other. Furthermore, Kondo shows that the soft element is not disposed between the chip (1) and lead frame (2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Ozawa by forming the soft element on the top surface of the chip and between the chip and the mold resin as taught by Kondo to protect the package from internal stress.

Ozawa and Kondo show all of the elements of the claims except the soft element being an elastomer or epoxy resin without a filler. It is well known in the art that encapsulant materials can be formed with or without fillers to form the encapsulant having a desired property (adhesive property, hardness property, etc.) However, Scranton et al. discloses (col. 17, lines 56-61) that an epoxy resin material may be formed without a filler to so that the resin has a putty-like property. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the soft element of Ozawa and Kondo by using an encapsulant material having no filler as taught by Scranton to form a soft element having a putty-like property.

Ozawa, Kondo and Scranton show all of the elements of the claims except the side surface of the two semiconductor chips being coplanar. Such a limitation is not patentably distinguishable over the cited art because two vertically stacked semiconductor chips being identical, or having the same size would have side surfaces that are coplanar. However, Nakayama et al. shows (fig. 2) a device having two semiconductor chips (30, 40) that are vertically stacked and have side surfaces that are coplanar. The chips allows mounting resin to extend to both sides of the chip to mount them to the substrate together [0111-0112]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Ozawa, Kondo and Scranton by forming the chips having coplanar side surfaces as taught by Nakayama to extend resin along both sides of the chip for mounting to a substrate.

In re claims 11 and 12, Kondo shows (fig. 2) that the surface comprises the entire surface that is contained by a single plane or that the surface comprises part of the entire surface that is contained by a single plane (as shown in figures 1 or 3).

In re claim 13, Ozawa discloses (col. 5, lines 50-65) that the encapsulant consists of an epoxy resin.

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (US 6,133,637) in view of Scranton et al. (US 6,099,783) and Nakayama et al. (US Pub. 2002/0004258 A1).

In re claim 14, Hikita et al. also disclose (col. 5, lines 8-55) a method of manufacturing a multi-chip package comprising: vertically stacking at least two semiconductor chips (14 and 16) on a substrate (lead frame 12a and 12b); the two chips having upper, lower, and side surfaces; bonding a bond pad (14b) on at least one of the at least two semiconductor chips to a bond finger (12b) on the substrate with a bonding wire (W); forming a soft element (26) on at least one side of at least one of the at least two chips; and encapsulating the semiconductor chips and the soft element using a mold resin (22). Hikita shows all of the elements of the claims except the soft element being an elastomer or epoxy resin without a filler. It is well known in the art that encapsulant materials can be formed with or without fillers to form the encapsulant having a desired property (adhesive property, hardness property, etc.) However, Scranton et al. discloses (col. 17, lines 56-61) that an epoxy resin material may be formed without a filler to so that the resin has a putty-like property. Therefore, it would

have been obvious to one of ordinary skill in the art at the time the invention was made to modify the soft element of Hikita by using an encapsulant material having no filler as taught by Scranton to form a soft element having a putty-like property.

Hikita and Scranton show all of the elements of the claims except the side surface of the two semiconductor chips being coplanar. Such a limitation is not patentably distinguishable over the cited art because two vertically stacked semiconductor chips being identical, or having the same size would have side surfaces that are coplanar. However, Nakayama et al. shows (fig. 2) a device having two semiconductor chips (30, 40) that are vertically stacked and have side surfaces that are coplanar. The chips allows mounting resin to extend to both sides of the chip to mount them to the substrate together [0111-0112]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Hikita and Scranton by forming the chips having coplanar side surfaces as taught by Nakayama to extend resin along both sides of the chip for mounting to a substrate.

In re claims 15 and 16, Hikita et al. shows (fig. 9) that the method includes forming the soft element on an entire surface of the upper chip (16) and a portion of the side of the lower chip (14).

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (US 6,133,637) in view of Scranton et al. (US 6,099,783) and Nakayama et al. (US Pub. 2002/0004258 A1) as applied to claim 14 above, and further in view of Kondo et al. (JP 63-240053 A).

In re claims 17-19, Hikita, Scranton, and Nakayama show all of the elements of the claims except the soft element contacting the entire surface of the an uppermost chip of the at least two semiconductor chips. Kondo discloses (abstract and fig. 2) a soft element (flexible material 9) formed on an entire upper surface and side surface of a chip (1). The soft element is formed between the chip and the mold resin (3) to protect the package from internal stress. The soft element also covers the bonding wire (5), the contact pad on the chip and the bond finger (4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Hikita, Scranton, and Nakayama by forming the soft element on the top surface of the chip and between the chip and the mold resin as taught by Kondo to protect the package from internal stress.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren

December 26, 2007

Primary Examiner